drop. As the power supply voltage continues to drop and reaches a level 13 a reset off (V.sub.RES) signal can be generated to turn off the integrated circuit. The time between the decreasing power supply voltage crossing level 12 and level 13, and indicated in the drawing as T.sub.NMI, should be sufficient to allow the microcomputer unit to execute the non-maskable interrupt.

Detailed Description Text - DETX (5):

Resistors 24, 26, 27, and 28 are all connected in series between power supply terminals V.sub.DD and 23. Resistors 24, 26, 27, and 28 serve as resistance means to provide a voltage divider having three different levels of outputs. The highest level output is connected to an input of a comparator 30. The other input of voltage comparator 30 is connected to node 25. Comparator 30 provides an output V reset which indicates when the power supply voltage V.sub.DD reaches a predetermined minimum voltage which is considered satisfactory for circuit operation. A second output from the power supply voltage sensor is taken from the junction of resistors 26 and 27 and coupled to an input of a voltage comparator 31. A second input of voltage comparator 31 is connected to reference output node 25. The output of comparator 31 provides a signal V NMI which would indicate a level of voltage at which a power fail condition exists and the integrated circuit should be providing for power shut-down. A third output from the power supply voltage sensor is taken from the junction of resistors 27 and 28 and is coupled to an input of a voltage comparator 32. The second input of voltage comparator 32 is connected to output reference node 25. The output of voltage comparator 32 provides V.sub.RESET which indicates power off as far as the circuit is concerned.

Detailed Description Text - DETX (14):

The constant voltage reference generator has been illustrated as useful in generating a power fail signal which can be used by a microprocessor or microcomputer to interrupt the processor and vector the processor to a power fail service routine and it will be understood that the FET voltage level detecting circuit can be used in conjunction with circuits other than microcomputers or microprocessors.

Claims Text - CLTX (6):

6. The voltage level detector of claim 5 further including a third voltage comparator having a first and a second input, the first input being coupled to the output of the constant voltage reference generator and the second input being coupled to the power supply voltage sensor at a point to provide a voltage lower in magnitude than provided to the second input of the second voltage comparator so that the first comparator can provide an output indicative of when the power supply reaches a first desired voltage in a power up situation, and the second comparator can provide an output indicative of when the power supply reaches a first predetermined voltage level in a power down situation, and the third comparator can provide an output indicative of

Fig. 1

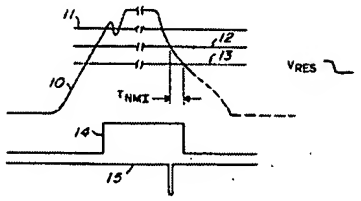
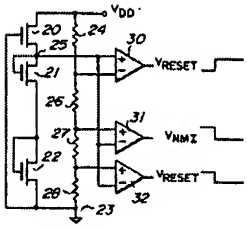
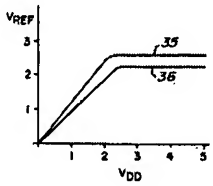


Fig. 2

Fig. 3





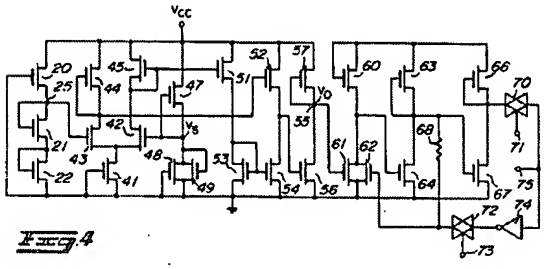


Fig. 4